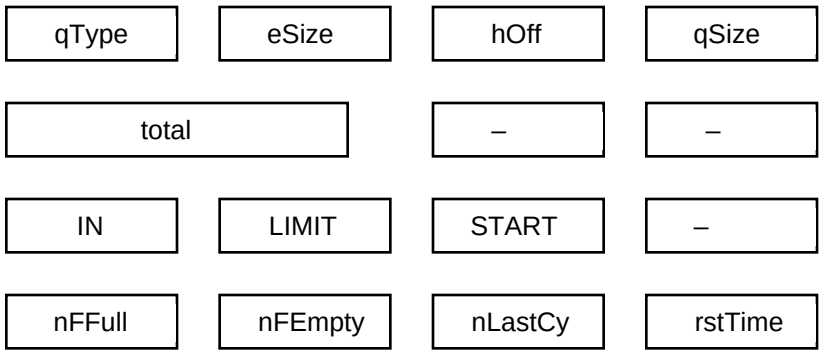
Clock Event Queue

For Clock Decoder board

Sep 6, 1989

The Clock Decoder board captures clock events and records them along with a 720 Hz time-stamp into a hardware fifo. In order to make this clock event data accessible to multiple users, the hardware fifo is read by a routine invoked from a Data Access Table entry, and its data is copied into a software circular buffer. This Clock Event Queue is implemented as a data stream and is therefore accessible via data requests using the data stream listypes.

The Clock Event Queue has the following format:

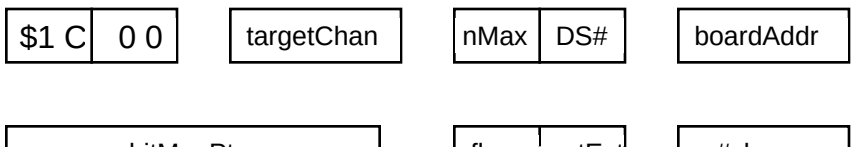


This layout is excerpted from the Data Stream Implementation document. The `qType`=1, the only currently supported queue type. The `eSize`=4, as the packets of data consist of a clock event# word followed by a time-stamp word. The `hOff`=24, the offset to the last 4 words which are clock event-specific data. The `qSize` is the total space used for the Clock Event Queue. The `total` long-word is a count of the total number of packets ever written into the queue.

The `IN`, `LIMIT`, and `START` words are used by the queue management routines associated with queue type 1. The `IN` word is the offset to the next available space in the queue. The `LIMIT` is the same as the queue size. The `START` word is the offset to the first packet in the queue. When the advancing `IN` word reaches `LIMIT`, it is reset to `START`.

The `nFFull` word is the number of times the fifo has been found with fifo full status. When this happens, the fifo is cleared. The `nFEmpty` word is the number of times the fifo has been found to be empty at the start of processing. The `nLastCy` word is the number of events that were found the last cycle that the fifo was accessed. The `rstTime` is the time-stamp value that was last read at the occurrence of a cycle reset event. It is used to adjust the time-stamps read to be relative to the time of cycle reset.

The Data Access Table entry format is as follows:



There are three jobs which can be done by this entry with the clock event data. The Clock Event Queue (as a data stream) records packets about each event that is read. A range of analog channels is updated with the most recent time-stamps for the corresponding events. A bit-map is updated with bits set to indicate the occurrence of the same range of clock events.

The `targetChan` is the base channel number of the range used to hold the time-stamp data, likely with the option enabled to store these time-stamp data relative to the time of the cycle reset event. The `nMax` byte is the maximum number of times the fifo is read while processing this DAT entry. The `DS#` byte is the data stream index used to identify the Clock Event Queue data stream according to the `DSTRM` table. The `boardAddr` is a word that gives the Clock Decoder board's fifo address in VME Short I/O space.

The `bitMapPtr` is a pointer to the base of the bit-map array which contains bits set to 1 whenever the corresponding event occurs. The bit-map may optionally be cleared at cycle reset time. The `flags` byte includes the following options:

bit#	option
7	1= enable cycle reset event logic
6	1= enable bit-map updating
5	1= enable bit-map clear upon cycle reset
4	1= longword bit-map array, 0= byte bit-map array
3	spare
2	spare
1	spare
0	spare

The cycle reset event# is specified by the next byte. It is only used if the cycle reset event logic is enabled. The `nChans` word is the number of channels starting at `targetChan` that are used to record the corresponding time-stamps. Events are processed in the range 00–n, where n= `nChans-1`. It is also used to give the range of events that are recorded in the bit-map table, if the bit-map is enabled.